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AIN INSULATOR FOR III-V MIS APPLICATIONS

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July 1, 1982 through June 30, 1984

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Building 410
Bolling Air Force Base
Washington, D.C. 20332

K.R. Elliott and R.W. Grant
Principal Investigators

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The use of AIN as an insulator for GaAs MIS structures was investigated. The AIN films were prepared by reactive evaporation in an ultra-high vacuum system. Aluminum from a MBE source was reacted with NH_3 from an effusion cell on a heated GaAs substrate. Several material preparation variables were investigated which included choice of substrate, substrate surface preparation, growth temperature, Al/NH_3 flux ratio, and deposition rate. The optimum AIN film growth parameters in terms of morphology and adhesion were found to involve use of thermally cleaned GaAs substrates, a 500-550°C substrate growth temperature, an effective NH_3 partial pressure of 5×10^{-5} to 1×10^{-4} Torr at the GaAs surface, and a growth rate of about 100Å/min. The AIN prepared in this manner was stoichiometric, polycrystalline, had the hexagonal wurtzite structure, and had no detectable oxygen or carbon contamination as determined by x-ray diffraction, TEM far infrared transmission, and in situ Auger electron spectroscopy.

The insulating properties of the AIN/GaAs MIS structures appeared to depend on preparation conditions. It was concluded from several studies that small amounts of undetectable residual oxygen contamination were most likely responsible for the observed variation in AIN conductivity. Complex C-V results were obtained

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for most AIN/GaAs MIS structures which most likely were influenced by large interface state densities, leakage, and charge storage effects. No definitive correlation between AIN/GaAs preparation parameters and interface state charge densities was obtained. Processes were developed to fabricate both gated diodes and MISFET's from AIN/GaAs samples. Electrical measurements on both devices provided no evidence that inversion was obtained and were consistent with the presence of large interface state densities. It was concluded that the AIN/GaAs interface is not suitable for MIS applications.

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1.0 INTRODUCTION

This is the final report for Contract No. F49620-82-C-0034; the contract is entitled "AlN Insulator for III-V MIS Applications." The development of a generally useful MIS technology for III-V semiconductors (e.g., GaAs) could have important digital and analog circuit applications. To be useful, the MIS insulator should have high resistivity and a low density of traps. In addition, the insulator/III-V interface should have a low interface state density. Most previous III-V MIS studies have utilized native oxides as insulators. For GaAs MIS in particular, the basic oxidation techniques that have been employed include anodic, thermal, and various types of plasma oxidation (extensive literature references are available, e.g., in Refs. 1-4). Studies of deposited oxides (and other materials) for MIS applications have also been reported. In most cases, when nonoxygen-containing deposited insulators have been studied, the GaAs substrate had several monolayers of native oxide present prior to insulator deposition. The chemical nature of native oxides which form on III-V semiconductors is complex in comparison, for example, to SiO_2 which is frequently formed on Si for MIS applications. Unfortunately, native oxides on III-V semiconductors are often poor insulators, have substantial trap concentrations, and have unacceptably large interface state densities.

In recent years, strong evidence in support of a defect model for Fermi level pinning at compound semiconductor intefaces has developed.[5-7] Although the atomic nature of the defects is not well understood, it is generally thought that the defects induce localized levels in the III-V semiconductor bandgap which can pin the Fermi level at the defect energy level. For GaAs it is observed that deposition of several metals onto the surface or exposure of the GaAs surface to oxygen causes the Fermi level to be pinned near mid-gap. The large densities of interface states which are frequently observed in GaAs MIS structures may be associated with the same defects which cause Fermi level pinning.

The minimization of intrinsic defects at III-V/insulator interfaces
could be a key factor for the development of a generally useful III-V MIS tech-
nology. One possibility that has been explored is the use of a lattice-matched
heterojunction to form the interface to GaAs. Members of the $Al_xGa_{1-x}As$ system
have been studied for this purpose in which the insulator was formed by either
introducing oxygen into the $Al_xGa_{1-x}As$ to make it semi-insulating[8] or by ther-
mally oxidizing the $Al_xGa_{1-x}As$.[9] One main difficulty encountered in attempting
to use $Al_xGa_{1-x}As$ as an MIS insulator is that the bandgap is too small to pro-
vide good insulating properties (the bandgap of AlAs is 2.2 eV).

It may not be necessary to use lattice-matched heterojunctions in order
to form a low interface state density MIS structure on III-V semiconductors (the
SiO_2/Si interface is not lattice-matched). From consideration of the defect
model of Fermi level pinning, it may be more important to choose an insulating
material which will minimize defect related interface levels. One possibility
is to utilize a wide bandgap III-V material. The isoelectronic nature of this
material could minimize interface states associated with both characteristic
defects (e.g., vacancies and antisites) and impurities. Only a few III-V mater-
ials would be suitable candidates for use as insulators. If one rules out
materials with bandgaps $\lesssim$ 3 eV and requires thermal stability of the material,
only AlN and BN are promising candidates.

AlN, which has a bandgap of 6 eV, is easier to prepare than BN. It has
been used as a successful capping material for GaAs ion implantation
studies.[10,11] Both of the substitutional impurities Al_{Ga} and N_{As} are electri-
cally inactive in GaAs and AlN is stable in vacuo to high temperatures. AlN is
also stable in air. The thermal expansion coefficients of AlN and GaAs are
nearly identical, and as a consequence, strain at the GaAs/AlN interface associ-
ated with thermal cycling is minimal and good adhesion is normally obtained.
For these reasons, a main goal of this program was to explore the concept of
using AlN as the insulator for GaAs MIS applications.

This report is organized into nine sections. Section 2.0 describes the
apparatus which was used to deposit AlN. Details associated with preparation of

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AlN films on GaAs substrates are given in Section 3.0. The characterization and
properties of the deposited AlN films are discussed in Section 4.0. Section 5.0
summarizes the electrical characterization of AlN films and AlN/GaAs MIS struc-
tures. The fabrication and test of AlN/GaAs MISFETs are described in Section
6.0. A program summary, Acknowledgements, and References are given in Sections
7.0, 8.0 and 9.0, respectively.

2.0 DEPOSITION APPARATUS

Thin films of AlN have been previously prepared by several techniques which include chemical vapor deposition,[12-17] dc and rf sputtering,[18-25] and reactive evaporation.[26-31] Chemical vapor deposition usually requires reaction temperatures that are too high to be compatible with GaAs substrates while most sputtering techniques have difficulty avoiding substantial oxygen incorporation into the AlN films and damage to the substrates. Reactive evaporation seems well suited for AlN film deposition on GaAs substrates.

Figure 1 shows a photograph of the bakeable stainless steel ultra-high vacuum (UHV) system which was used for AlN depositions in this program. The UHV conditions were obtained by both ion- and cryo-pumping. After bakeout and prior to initiation of AlN deposition, the system base pressure was in the low 10^{-9} Torr range. The system included a load lock in order to increase sample throughput and maintain vacuum integrity. By using this load lock, the cycle time of the system was ≈ 2 h per sample. In addition to providing a more efficient means to optimize the deposition process, the load lock improved the ability to decrease background impurity levels.

Temperature control of the GaAs substrate is an important factor in the AlN deposition process which is discussed in Section 3.2. In addition substrate temperature control is required for thermal cleaning of GaAs surfaces. A Varian MBE 2 in. diam heated substrate station was used to obtain substrate temperature control.

An NH_3 effusion cell was constructed from a conventional stainless steel 2-3/4 in. cross which was attached to the UHV deposition chamber by a solid copper gasket. The NH_3 was directed toward the substrate through a ~ 1 mm diam hole in the Cu gasket. By monitoring the NH_3 pressure in the cell, it was possible to control the NH_3 flux at the sample surface. The cell volume was ~ 200 cm^3; pressure in the cell was monitored by a thermocouple gauge and was typically 10^2-10^3 μ. Cell pressure was regulated by a leak valve. During AlN deposition the ion-pump was valved off to prevent overloading by NH_3 and the

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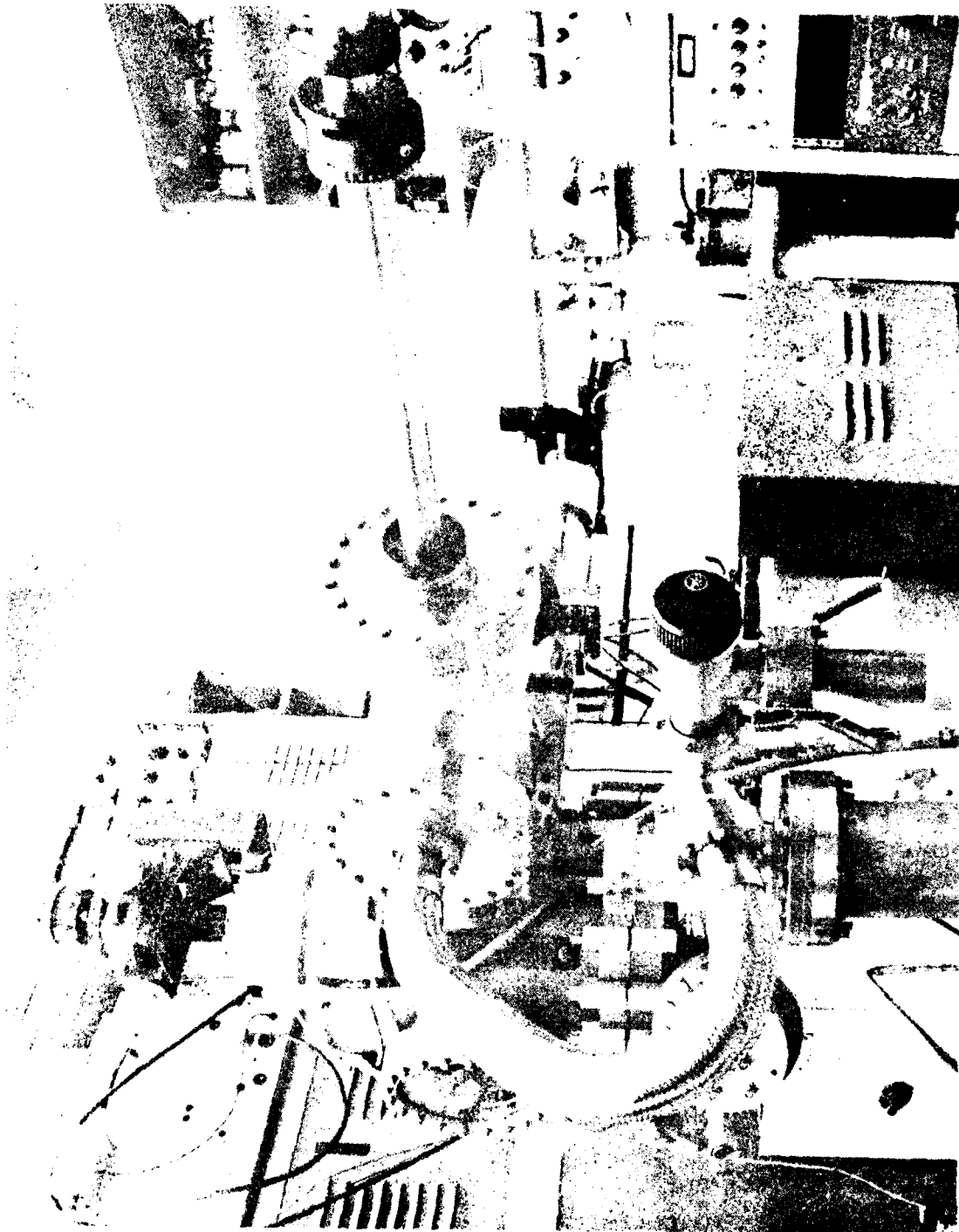
Fig. 1 AlN deposition apparatus.

deposition chamber was only cryo-pumped. Chamber pressure during deposition was typically in the high 10^{-5} Torr range. The source to substrate distance was about 6 in.

A commercially available Physical Electronics Industries, Inc. (PHI) MBE source was used to obtain a controlled and stable Al flux. The load lock mentioned above substantially helped to minimize Al source contamination problems. The Al source to substrate distance was about 8 in. A quartz crystal deposition monitor was used to calibrate the Al flux as a function of source temperature; also, the AlN growth rate in substantial excess NH_3 flux (as observed by film color changes) provided an additional monitor of the Al flux.

An Auger electron spectroscopy (AES) analyzer was attached to the UHV system which made it possible to monitor the GaAs surface composition prior to deposition and the composition of the deposited AlN.

3.0 ALUMINUM NITRIDE PREPARATION INVESTIGATIONS

As described in Section 3.6, a number of approaches were tried to produce clean aluminum nitride-gallium arsenide interfaces. The most successful approach was the use of reactive evaporation to deposit smooth continuous films of AlN on GaAs substrates. In this section the results of studies made on the growth of these films are reported. In Section 3.1 the procedures used to prepare GaAs substrates for deposition and the properties of substrates used in the course of these studies are described. Section 3.2 describes the dependence of film formation on temperature and the effects of changing the reactant species flux ratio. Section 3.3 describes the use of an As source in an effort to change the surface properties prior to deposition. In Section 3.4 the effects that small amounts of residual contamination can have on the macroscopic properties of the films are discussed. In Section 3.5 the results of studies on crystallographic orientation of the substrate material are described. In Section 3.6 the results of other approaches to form AlN/GaAs structures are discussed and in Section 3.7 a summary is presented of the conditions which seem to give optimal AlN films on GaAs.

3.1   Substrate Material and Preparation

Substrates were obtained from a number of different sources. At the beginning of the program p- and n-type substrates grown by horizontal Bridgman were used for the source material. Subsequent studies utilized liquid encapsulated Czochralski (LEC) grown n^+ and n^- material, undoped semi-insulating material, and undoped p-type material. In addition, epitaxial layers grown by molecular beam epitaxy in a Varian Gen-II MBE system were studied. These layers were coated with a layer of elemental As following growth for an oxygen and contaminant free transfer to the AlN deposition system. Regrowth of GaAs on such surfaces has been shown to be relatively defect free.

No substantial difference in the quality of the films was determined in any of the measurements described later in the report between different types of

substrates. LEC substrates were preferred for a number of reasons over the horizontal Bridgman substrates used initially in the program. First, since well characterized LEC material was internally available at Rockwell, some control over substrate quality could be assured. Secondly, the LEC material which was available had a superior surface finish to the available Bridgman material. In general, the LEC material had fewer scratches, fewer precipitates, and lower densities of surface defects than the Bridgman material.

The MBE layers exhibited inferior surface morphology to the bulk material. Oval defects are presently unavoidable even in state-of-the-art MBE layers. The occurrence of such defects gives rise to pinholes in the AlN layers which can lead to leakage in the MIS structures.

A cleaning procedure similar to that used for standard MBE growth was used to prepare the substrate for AlN deposition. Auger measurements on surfaces prepared by using this procedure indicate that the surface is free from residual carbon contamination. As discussed in Section 3.4 such contamination can lead to morphological inhomogeneities in the AlN films. These cleaning procedures consisted of 1) degreasing the GaAs surface with conventional solvents, 2) attaching the GaAs substrate to a Mo substrate holder with In and 3) spin etching the GaAs with a $NH_4OH:H_2O_2:10H_2O$ solution. The substrate is rinsed with ultra-high purity water and spun dry. The substrate is inserted into the vacuum system loadlock within 30 s of the final step. Any residual water on the substrate holder is cryo-pumped in the loadlock. The GaAs substrate prepared in this fashion is carbon-free and suitable for heat cleaning.

3.2 Dependence of Film Growth on Temperature and Flux Ratio

AlN is deposited on GaAs by using reactive evaporation. In this process one of the sources for the deposition consists of a normal MBE Knudsen cell while the second source consists of an ammonia (NH_3) effusion cell. A chemical reaction between the ammonia and aluminum results in the formation of an AlN film on a heated substrate. Normally, the reaction occurs at the surface of the

substrate and it is necessary to heat the substrate as evidenced by the temperature dependence of film formation.

In the course of this investigation the conditions necessary for optimal film growth of AlN on GaAs were determined. A number of variables in principle can affect the growth of AlN films. These include the temperature of the substrate, the flux ratio of the constituent species, the type and quality of the substrate material, the rate of deposition, and the presence of contaminating species. Each of these was found to be important to some extent, however, the dependence of film formation on temperature and flux ratio is probably the most important.

Following insertion into the vacuum system, the substrate was normally heated to a temperature between 550°C and 600°C to remove residual oxygen and carbon from the surface. In some cases the surface was heated as high as 700°C prior to deposition. In other cases the sample was not heated above 500°C. In still other cases the film was heated to 650°C for cleaning and cooled to temperatures below 550°C for growth. At the same time the ammonia flux was altered by an order of magnitude and the AlN growth rate by roughly a factor of 5. In the early stages of the program the ammonia was evacuated from the system using an ion pump to prevent accumulation of hydrogen and ammonia in the vacuum system during growth. Since ion pumps are easily loaded by ammonia the growth rate, film thickness, and flux ratio were limited accordingly. In the course of the program a cryo-pump was added to the system which permitted a much larger range of growth rate and flux ratio and much better control over these parameters.

During the course of the program approximately 100 AlN layers were deposited on GaAs substrates under different conditions. The results were not always reproducible in terms of electrical behavior and surface morphology, however, the following observations could be made in different temperature ranges.

Films grown at temperatures greater than 625°C principally consisted of relatively pure AlN although small amounts of Ga and As could be observed in the Auger spectra even for films as thick as 1000A. Relatively high growth rates

(200A/min) could be obtained for a modest NH_3 flux which corresponded to an effective partial pressure of $\sim 10^{-5}$ Torr at the GaAs surface. The films had a granular structure as described in Section 4.4 and did not adhere well to the GaAs surface. Films which were thicker than 3000-5000A had a tendency to lift and peel and films as thin as 1000A peeled when annealed at temperatures above 700°C.

Films grown below 575°C with the same flux ratio contained free aluminum as determined by visual inspection and Auger analysis. The exact ratio of aluminum-to-aluminum nitride could be expected to vary from run-to-run. When the effective ammonia pressure was raised to roughly 10^{-4} Torr pure aluminum nitride could be obtained. The adhesion of the AlN was substantially improved and no peeling or lifting was observed. The morphology was considerably smoother as demonstrated by observing scattered light from the surface and as observed by SEM (Section 4.4). Typical growth rates ranged from 50 to 150A/min. It was possible to maintain pure aluminum nitride to temperatures as low as 400°C. Below this temperature AlN can probably be deposited by increasing the NH_3 flux, however, it becomes increasingly difficult to prevent residual oxygen and water in even the highest purity ammonia available commercially from reacting with the aluminum to form aluminum oxides.

When the GaAs surface is heated above 625°C and the substrate is cooled below 575°C for the AlN deposition, the surface again shows the granular morphology described above. The same result is obtained if the sample is briefly exposed to the Al flux in the absence of the ammonia flux.

Between the temperatures of 575°C and 625°C films were normally obtained which resembled either of the two cases described above. The results in this temperature range were not reproducible most likely because it is extremely difficult to reproduce exact flux ratios and temperatures on a run-to-run basis.

The observed behavior can be explained if it is assumed that the surface has deteriorated by formation of free Ga under some circumstances. Excessive heating of the GaAs surface during heat cleaning, reaction with free Al prior to reaction with the ammonia or an insufficient ammonia flux would lead to

the formation of a Ga-rich phase at the GaAs surface. By using such a model one could predict poor adhesion and morphology from such layers. This interpretation is supported by the appearance of the GaAs surface following an etch of the deposited AlN. The GaAs surface has a cloudy appearance following such an etch indicating that some kind of chemical reaction or thermal decomposition has occurred.

3.3   Dependence on As Flux

In an effort to reduce surface degradation as described in the preceding section and also to help eliminate thermally induced surface states, an As source was added to the system. As a result it was possible to grow a number of different structures in situ, including GaAs/AlAs/AlN. The results of these studies are described in Section 3.6. No perceptible difference was observed in the physical or electronic properties of the structures with As flux present compared to the normal structures. In fact, as discussed in Section 5.3, no strong correlation between any deposition parameter and interface state density was observed.

3.4   Surface Contamination

In the course of this investigation, it was found that the growth of AlN was extremely sensitive to contamination and damage of the surface even when such contamination or damage was not necessarily observable by Auger spectroscopy or obvious from optical inspection. Following growth, damage or contamination resulted in a color change of the films in the region where the contamination or damage occurred. Because pure AlN is transparent in the visible and the film color is due to optical interference, this color change can be associated with minute changes in the thickness or refractive index of the films. Figure 2 shows an SEM micrograph of a region where contamination had obviously occurred. In this case the pattern indicated that the nonuniformity was associated with incomplete and nonuniform rinsing of the GaAs surface following the final surface etch. The nonuniformity in this case leads to a

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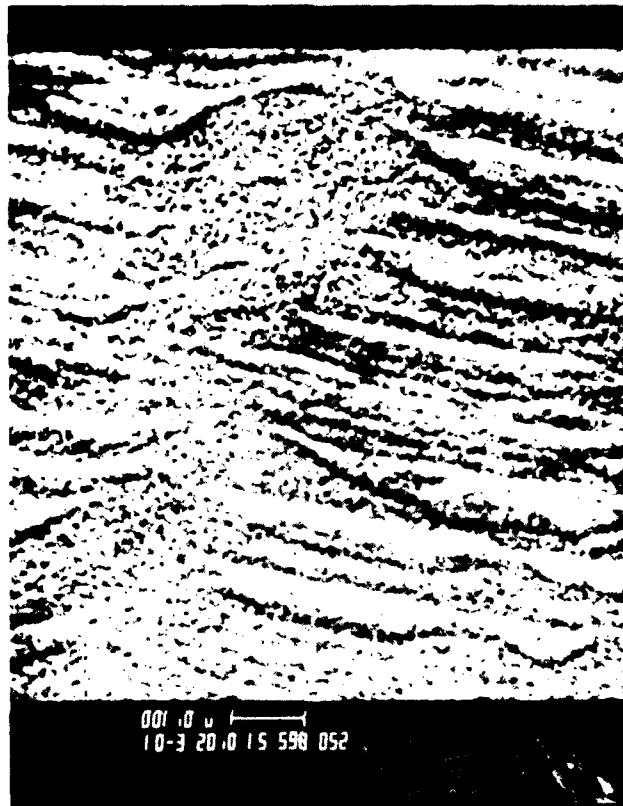
Fig. 2 SEM micrograph of AlN/GaAs film with surface initially
contaminated by carbon.

thickening of the layer in the neighborhood of the contaminating species. Simi-
lar effects are observed at the edge of the sample where the sample had been
handled with tweezers during mounting prior to etching and in regions where car-
bon from the electron gun of the AES had been deposited _in situ_. Such patterns
were frequently observed even when AES gave no indication of contaminating spe-
cies and when the sample appeared specular visually. The phenomenon is probably
associated with nucleation of AlN on the semiconductor surface.

Another observed phenomenon was that small amounts of In from the sample holder on occasion would react with the AlN films destructively to form an In-Al alloy. The reaction would proceed from the edge of the wafers inwards as In evaporated onto the edge of the wafer. It was possible to control this degradation by carefully cleaning excess In from the sample holder prior to etching the sample. The reaction also proceeded more slowly with higher ammonia flux.

3.5   Crystallographic Orientation

Most of the AlN layers were deposited on GaAs substrates with (100) orientation. Because the orientation of the substrate was possibly an important parameter in determining the quality of the layers and the interface, the growth of AlN on substrates with (111)A and (111)B oriented GaAs surfaces was also investigated. These surfaces were particularly interesting because of a possible superlattice match between AlN and GaAs. If one compares the lattice spacing of GaAs and AlN one finds that four AlN lattice spacings (4 × 3.1114 = 12.4456A) matches within four percent the distance in three GaAs lattice spacings (3 × 3.9980 = 11.9939A). Hence, one might expect favorable properties for deposition on the (111) surfaces. The layers grown on the (111) surfaces showed a surface morphology indistinguishable from those grown on (100) surfaces. The films also had a tendency to peel. In addition, no x-ray diffraction pattern was observed from these films. As a result there was no indication that deposition on (111) surfaces showed any improvement in film quality.

3.6   Alternate Approaches to Forming AlN/GaAs Structures

In addition to using reactive evaporation to form AlN/GaAs structures, other methods for forming this type of structure were also investigated. The installation of an As source enabled growth of AlAs layers; attempts were made to convert these layers to AlN. It was also attempted to convert As-overcoated AlAs layers to AlN layers. A number of different N sources were used in the reactive evaporation process.

Because the ordinary deposition of AlN leaves an interface which is not lattice-matched to the substrate and which at least initially had a large

density of interface states, the growth of structures which were more likely to have less strain and which might have a lower density of interface states was attempted. Initially growth of an AlN/AlAs/GaAs structure was tried. These structures electrically were similar to the AlN/GaAs structures described previously and were more difficult to process since AlAs is less stable chemically than AlN. An attempt was made to take an AlAs/GaAs structure and react the AlAs in situ with ammonia to form AlN. Within the temperature and pressure range available in the vacuum system, no substantial reaction to form AlN occurred. Auger analysis indicated the presence of a few monolayers at most of reacted N on the surface of the AlAs. In addition a layer of AlAs grown in a Varian Gen-II MBE system which had been overcoated with As to protect the layer against oxidation was reacted with ammonia in a furnace at temperatures from 600°C to 900°C. In this case, the ammonia overpressure was roughly a factor of 1000 higher than in the previous case. An initial reaction was observed as low as 600°C in some cases, however, the reaction was nonuniform and did not proceed to completion until temperatures were in excess of 900°C. The films which were formed had poor morphology and were clearly not suitable for device applications.

The use of different nitrogen sources other than ammonia was also investigated. Because pure nitrogen gas of higher purity than ammonia is readily available, these efforts concentrated on using pure nitrogen as a source material. Stoichiometric AlN could not be formed by using N_2 gas in our system. Attempts were made to create activated nitrogen species by creating an electrical discharge in the nitrogen. Growth of AlN with this source was also not possible.

3.7   Summary of Optimum Growth Parameters

In this section a summary of the growth parameters which gave the best films is presented. The criteria for judging the best films were film morphology and film adhesion. Not considered here are the electrical properties or interface properties as discussed in later sections. The electrical properties were not always sufficiently reproducible from deposition to deposition to say

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that one procedure was better than another. However, it was possible to reproducibly deposit films with good morphology and adhesion, essential properties for a viable process technology.

1. GaAs substrate material was degreased by using a standard solvent cleaning procedure as described in Section 3.1.

2. The substrate was mounted on a Mo substrate mounting block with molten In. The total amount of In not covered by GaAs was minimized.

3. The substrate holder and substrate are etched on a spinner with a spray of 10:1:1 $H_2O:H_2O_2:NH_4OH$ and rinsed with ultrahigh purity H_2O (20 megohm-cm or better). The sample is spun dry to remove excess water from the GaAs surface.

4. The sample is immediately inserted into a load lock of the vacuum system. Residual water is removed by pumping with a sorption pump.

5. When the load lock has been pumped below 10^{-6} Torr the sample is transferred to the main deposition system with base pressure roughly 5 to 9×10^{-9} Torr.

6. The sample is outgassed at 200-300°C.

7. The surface oxide on the sample is desorbed at approximately 600-625°C.

8. The Al flux is adjusted for a growth rate of approximately 100Å/min.

9. The NH_3 flux is adjusted for an effective partial pressure of 5×10^{-5} to 1×10^{-4} Torr at the sample surface.

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10. The substrate temperature is lowered to 500-550°C.

11. Growth is initiated. During growth a cryopump was used to remove any excess ammonia, hydrogen, and residual impurities in the ammonia which may accumulate in the chamber during growth.

4.0 AIN PROPERTIES AND CHARACTERIZATION

AlN films produced in this program were characterized by a number of techniques which included AES, x-ray diffraction, TEM, SEM, XPS, far infrared transmission and Raman spectroscopy.

4.1   Auger Electron Analysis

The Auger electron spectrometer (AES) attached to the growth apparatus enabled in situ characterization of the AlN film purity. A typical Auger electron spectrum of an AlN film immediately following growth on a GaAs substrate is shown in Fig. 3. The predominant peaks in the spectrum are associated with Al at 57 eV and N at 381 eV. Oxygen and carbon are not detectable in the spectrum, which indicates that the films have good purity. For the spectrum shown in Fig. 3, the composition of the stoichiometric AlN is estimated to be [Al]/[N] = 0.94 ± 0.15. The oxygen content is estimated to be less than 0.2% from the same spectrum.
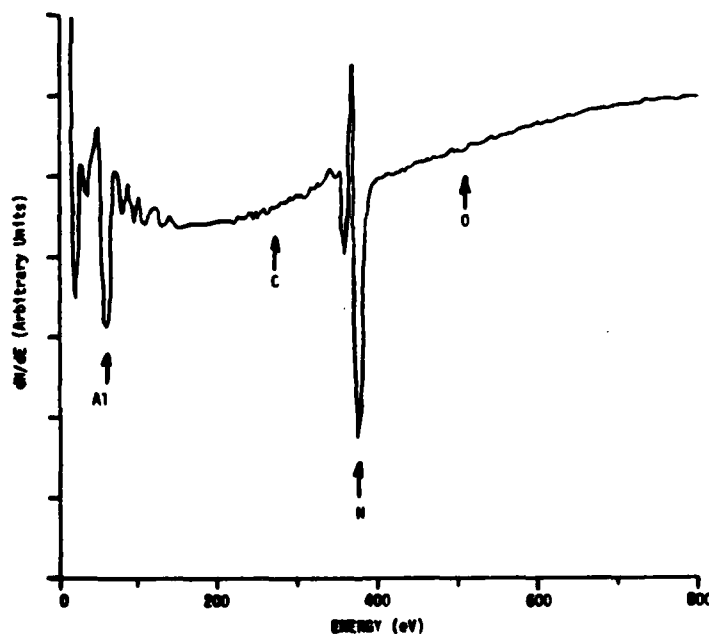
Fig. 3   In-situ Auger electron spectrum of AlN film grown on GaAs. Note the absence of oxygen and carbon in the spectrum.

Occasionally, the presence of Ga and As was observed in the films, particularly for films grown at higher temperatures. The presence of other elements in the AlN films was not detected.

4.2   X-Ray Analysis

X-ray diffraction data were obtained from samples deliberately grown relatively thick for this purpose and removed from the substrate. Both specular (~1.5 μm thick) and nonspecular (~ 0.5 μm thick) films prepared as discussed in section 3.2 were analyzed. The most definitive data were obtained with a Gandolfi camera. This camera rotates a millimeter diameter sample around two axes inclined 45° to each other to generate a series of random orientations. In this way it simulates an ideal powder containing randomly oriented grains and produces a powder pattern photograph like that obtained with an ordinary Debye-Scherrer powder camera. A Gandolfi photograph of a nonspecular (~ 0.5 μm thick) AlN film is shown in Fig. 4. It agrees well with published data[32] and was indistinguishable from the specular film result. The crystal structure is the wurtzite type, which is hexagonal with space group $P6_3mc$. Lattice parameters measured from the photograph are a = 3.12 ± 0.01A and c = 4.98 ± 0.01A which agree with published values[32] within the indicated experimental error. The diffraction maxima in the photograph are rather broad; the $K\alpha_1$ - $K\alpha_2$ doublet is not resolved. The line broadening may result from strain or small grain size or both. Either a single crystal or polycrystalline sample would yield the Gandolfi data just described. To characterize the films better, Laue photographs were also taken for the specular ~ 1.5 μm thick sample removed from the substrate. No back reflection Laue data could be obtained. The transmission Laue photograph shows incomplete rings with the same Bragg angles as the maxima on the Gandolfi photograph. This implies that the film is polycrystalline and fine-grained but with some preferential orientation (or texture). A single crystal film or one with large grains would yield a typical Laue pattern of discrete reflections. A polycrystalline film with fine randomly oriented grains would result in an ordinary powder pattern with complete rings on the flat film of the Laue film cassette. Neither of these results was obtained. Nor could
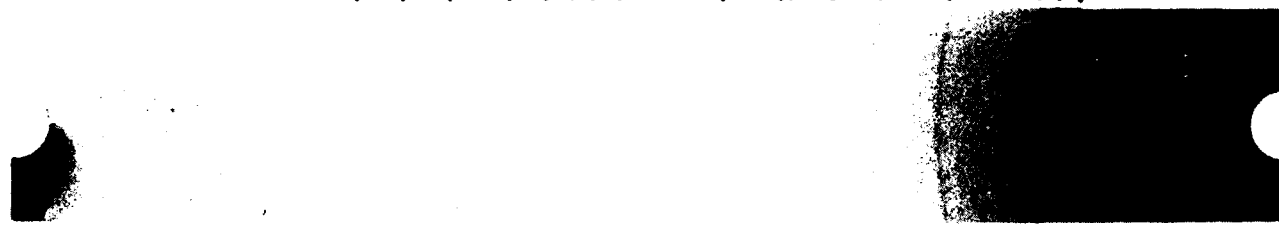
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Fig. 4 Gandolfi x-ray photograph of AlN film.

any single crystal or powder pattern be obtained with a scintillation-detector-equipped diffractometer. On the basis of the Gandolfi and transmission Laue data, we conclude that the films have a textured polycrystalline structure similar to that found by Alexandre et al.[31] in AlN films prepared by a similar process.

4.3   TEM Analysis

A specular AlN film of $\sim 10^3$A thickness was examined by transmission electron microscopy (TEM). The thin-film specimen was prepared by first mechanically thinning the GaAs substrate to a thickness of approximately one mil. The thinned substrate with the AlN film intact was then reduced to electron transparency by chemical polishing in a solution of equal parts of water, hydrogen

peroxide, and ammonium hydroxide. The GaAs dissolved more rapidly than the AlN in this solution, and the polishing was halted as a few holes developed in the substrate. These holes were covered by the AlN film which could be observed in the TEM. The AlN film was found to be polycrystalline, with a crystallite size of approximately 5 to 10 nm, Fig. 5a. Selected area electron diffraction revealed a fairly random orientation of the crystallites, Fig. 5b, with apparently little influence of the GaAs on the orientation of the AlN. The apparent difference in film texture and crystallite size as compared to the x-ray analyses (Section 4.2) may be associated with the film thickness.

4.4   SEM Analysis

As indicated above, the films are composed of crystalline stoichiometric AlN. Scanning electron microscopy (Fig. 6) shows that AlN films grown with proper substrate preparation (see Section 3.1) have granular morphology with features approximately 1000A across. It is possible that these features are individual crystallites of AlN. Comparison of SEM, TEM, and x-ray analyses suggests that AlN crystallite size may vary from run to run.

An SEM micrograph of a relatively thick (~ 1.7 μ) AlN film grown on a GaAs (100) substrate is shown in Fig. 7. The sample was broken and mounted on edge to reveal a cross-section. Good control of thickness uniformity is observed. A columnar type of growth is suggested for the AlN film.

4.5   XPS Analysis

X-ray photoemission spectroscopy (XPS) was used to analyze the surface of a thick ($\simeq 10^3$A) AlN film grown on GaAs (100) in the reactive evaporation deposition system (Section 2.0), and subsequently transferred in air into the XPS apparatus. A spectrum is shown in Fig. 8. The substantial O1s signal observed in this spectrum indicates that $\simeq$ 10A of the surface is oxidized by air exposure. Thus, it may be important to cap the AlN with a metal before removing it from the growth system to prevent traps from forming due to the presence of the thin oxidized AlN layer.

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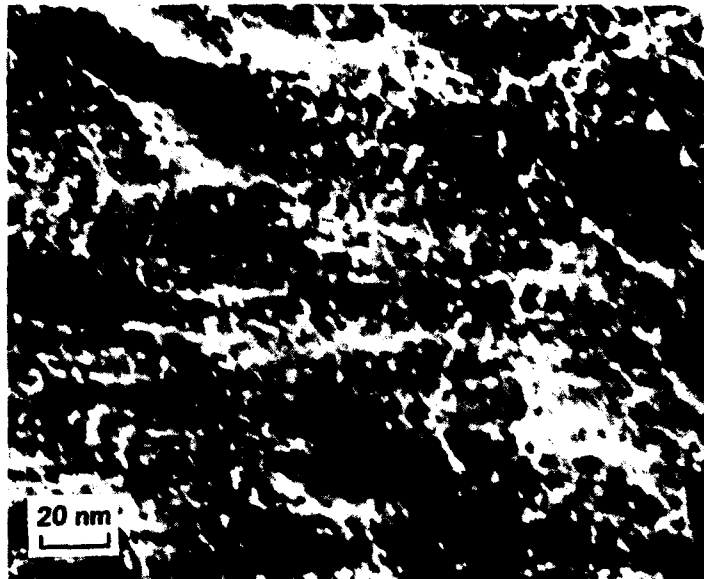
a)
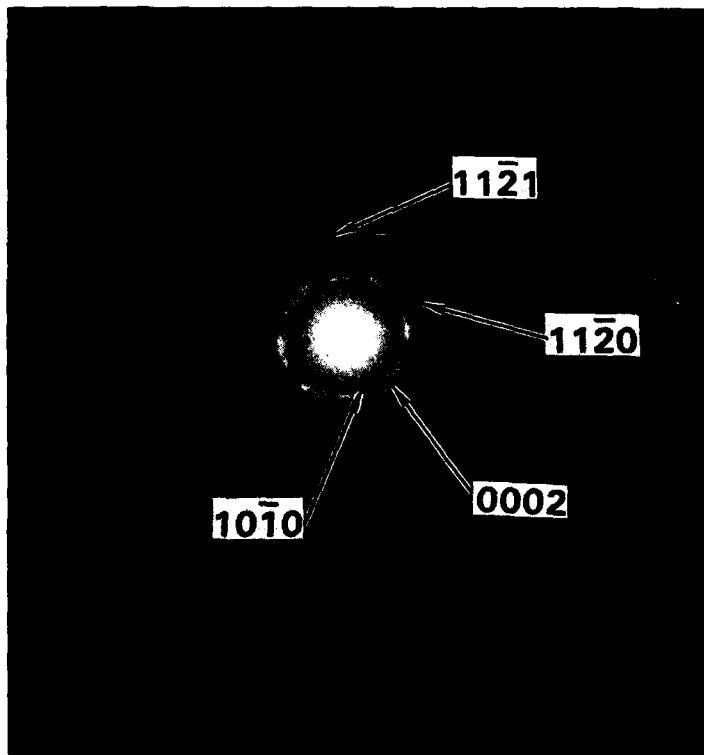
b)

Fig. 5 a) TEM micrograph of AlN film which shows fine grain structure, and
       b) associated selected area electron diffraction pattern.

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001 .0 u
10-3 20.0 15 598 041

Fig. 6   SEM micrograph of AlN/GaAs film which shows granular morphology.

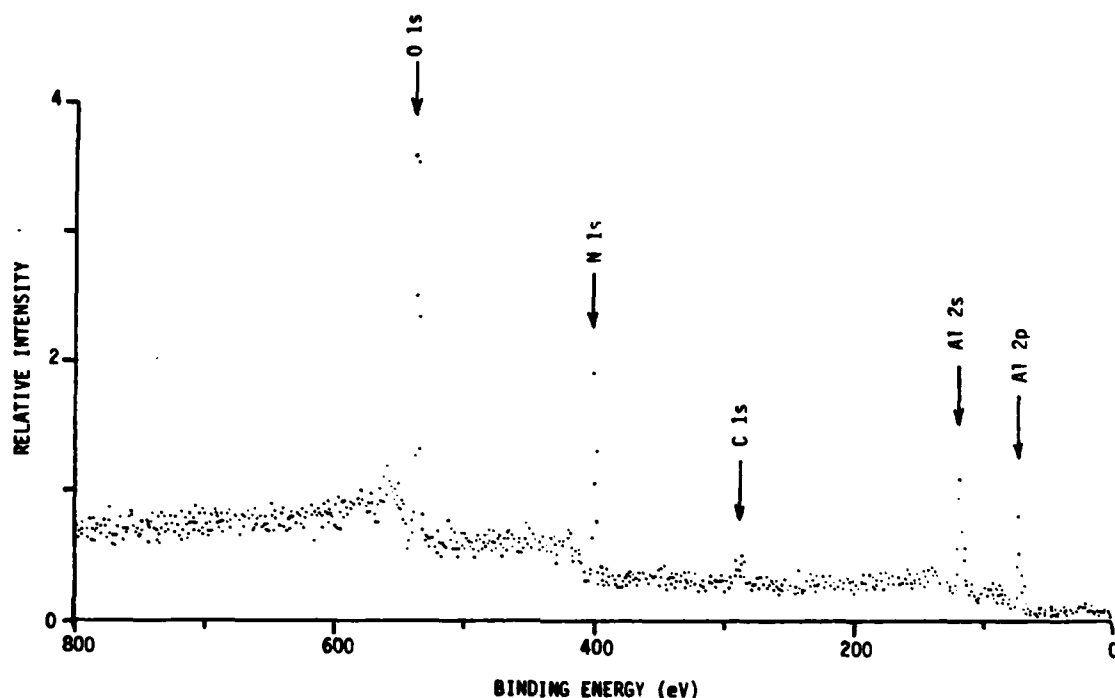Fig. 7   SEM micrograph of AlN/GaAs sample cross-section.

22

Fig. 8 XPS spectrum of AlN surface after several hours of air exposure.

The stability of a GaAs (100) substrate to NH_3 exposure was investi-
gated by XPS. The substrate was thermally cleaned ($\sim 550°C$) in the UHV sample
preparation chamber of the XPS system. This chamber was backfilled with NH_3 to
$\sim 4 \times 10^{-5}$ Torr and the clean substrate was heated for 5 min at 200°C, 425°C,
500°C and 550°C, respectively. Following each heat treatment, the substrate
surface was chemically analyzed by XPS. No evidence of nitride formation or of
any other surface chemical reaction was observed. In addition, no change in
surface band bending as a result of NH_3 exposure was noted.

The XPS sample preparation chamber was equipped with a Low Energy
Electron Diffraction (LEED) apparatus. LEED was used to characterize AlN layers
deposited _in situ_ on GaAs (100) and GaAs (111)B substrates. The GaAs (100) sub-

strate was thermally cleaned and exhibited a LEED pattern. The sample preparation chamber was backfilled with NH_3 to $\sim 10^{-4}$ Torr and Al as evaporated (~ 0.7Å/s) onto the heated ($\sim 400°C$) substrate to form an AlN layer about 45Å thick. Oxygen was observed as a contaminant in the layer and the oxygen/nitrogen ratio was ~ 0.1. No LEED pattern was observed from this surface. A similar procedure was used to deposit a somewhat thicker AlN layer onto a GaAs (111)B substrate; this substrate had been cleaned by sputtering (1 keV Ar^+) and annealing to obtain a LEED pattern. Following AlN deposition, no LEED pattern was observed.

XPS was also used to obtain a rough estimate of the relative energy band positions of AlN and GaAs. The GaAs (100) substrate with the ~ 45Å layer of AlN (described in the preceeding paragraph) was used for this purpose. the XPS spectrum of the valence band region (0 to 15 eV) for this sample is shown in Fig. 9. The solid curve in the figure is the expected position and intensity of the highest lying GaAs valence band as determined by comparison with published GaAs spectra[33] and normalization to the As 3d line intensity. It might be expected that the XPS experimentally observed valence band density of states for AlN would resemble that of GaN (see Ref. 34). The rapid signal increase at ~ 2.8 eV below the GaAs valence band maximum (0 eV on the binding energy scale) is most likely associated with the AlN valence band maximum. This would place the valence band maximum of AlN ~ 2.8 eV below that of GaAs and the conduction band minimum of AlN ~ 1.8 eV above that of GaAs.

4.6   FIR and Raman Analysis

The properties of the AlN films and the GaAs substrate were investigated with far infrared transmission (FIR) and Raman scattering spectra. Figure 10 shows a typical transmission spectrum of an AlN layer on a bulk GaAs substrate between 500 cm^{-1} and 1000 cm^{-1} (20 μm and 10 μm, respectively).

The GaAs substrate is relatively transparent in this spectral range, except for a two phonon peak at 520 cm^{-1}. The spectrum shows peaks at 610 cm^{-1}, 650 cm^{-1} and 671 cm^{-1}, which corresponds to lattice TO phonons in AlN. These values compare with 610 cm^{-1}, 655 cm^{-1} and 667 cm^{-1} for results obtained on bulk
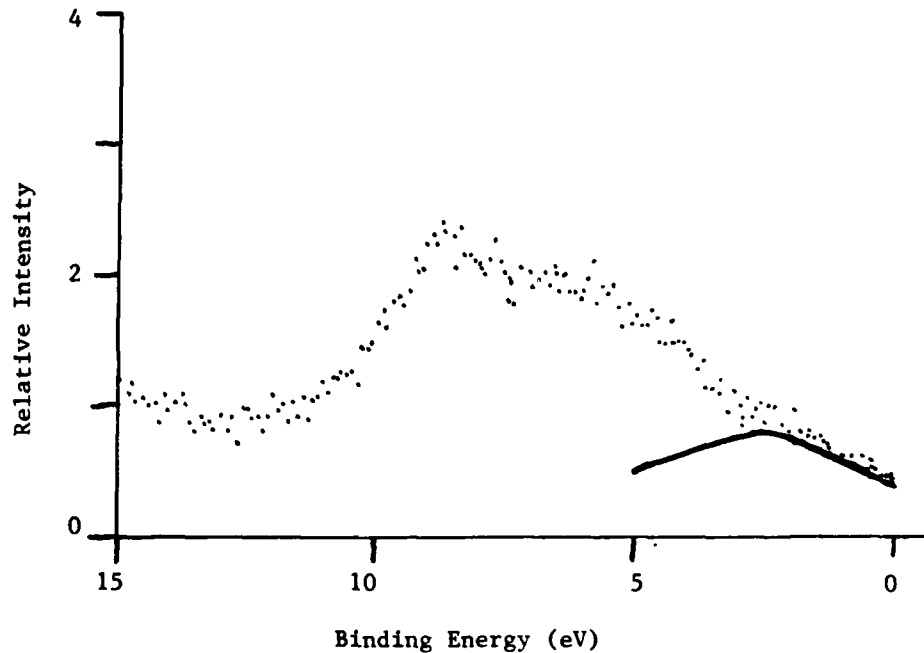
MRDC41116.2FR

Fig. 9 XPS spectrum of valence band region for a ~45A thick
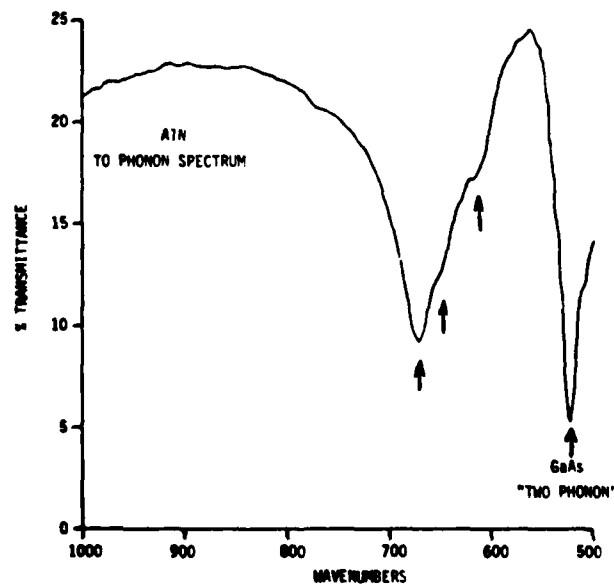AlN layer on a GaAs (100) substrate.

Fig. 10 Infrared absorption spectrum of AlN film grown on GaAs substrate which
shows transverse optical modes (marked by arrows) associated with AlN.

AlN crystals.[35] These results support the Auger and x-ray analyses which indicate the films consist of stoichiometric crystalline AlN.

The Raman spectra of the underlying GaAs substrate was also investigated (see Fig. 11). Such spectra have previously been interpreted in terms of strain at the insulator/GaAs interface.[36] The GaAs LO phonon mode is observed at 291 cm^{-1} with a width of 7 cm^{-1}. This can be compared with a width of 5 cm^{-1} for a clean GaAs surface. Thus, strain related broadening of the Raman line is minimal for the AlN deposited on GaAs by reactive evaporation.

GaAs Raman Spectrum

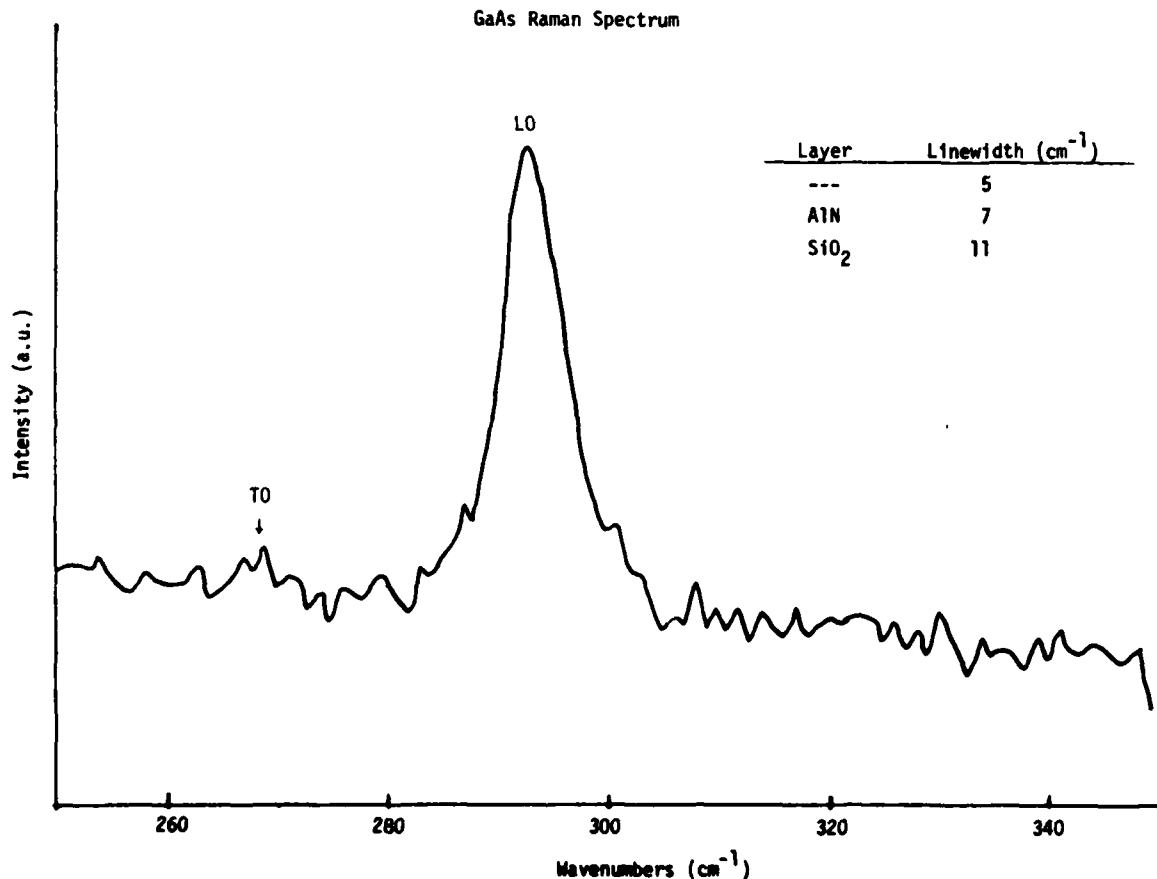| Layer	Linewidth (cm^{-1})
---	5
AlN	7
SiO_2	11

Fig. 11   Raman spectra of AlN/GaAs sample. As noted in figure the GaAs LO phonon mode for a clean GaAs substrate was 5 cm^{-1}, for the AlN/GaAs sample was 7 cm^{-1} and for a SiO_2/GaAs sample was 11 cm^{-1}.

5.0 ELECTRICAL PROPERTIES OF AlN FILMS ON GaAs

5.1   Frequency Dispersion

To determine the dielectric properties, variable frequency C-V meas-
urements have been made for AlN films grown on degenerately doped GaAs sub-
strates. The thickness of the films was determined optically and found to be
inversely proportional to the capacitance as expected. The results of these
measurements are shown in Fig. 12. At low frequencies, the dielectric constant
of the insulator increases rapidly. The high frequency dielectric constant
corresponds to a value of 8, close to that reported for bulk AlN. A number of
explanations can account for this behavior; the most likely is that the disper-
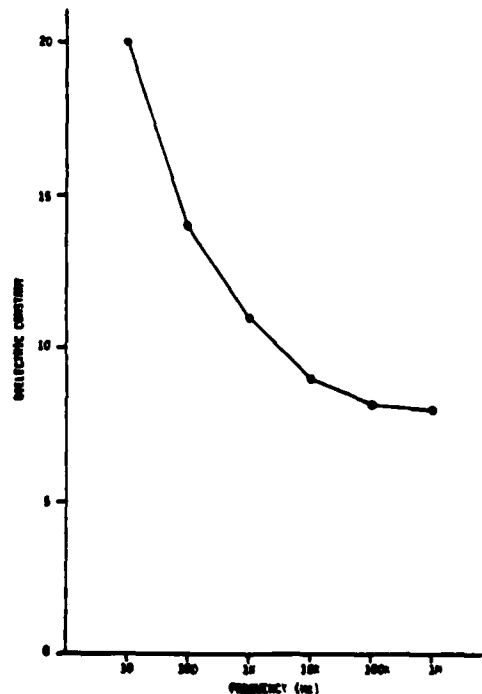sion results from conduction associated with trapping centers in the insulator.

Fig. 12 Dispersion of dielectric constant for AlN film
on n+ GaAs substrate.

The conduction in the AlN films is complex and depends on film preparation and history. The insulating properties of the films will be discussed in the following section.

5.2 Conduction Dependence on Preparation of AlN Films

The insulating properties of the AlN/GaAs structures appeared to vary with the preparation conditions. Films were obtained which were highly insulating on some occasions. On other occasions the films were sufficiently conducting to make conventional C-V analysis of the structures impossible to interpret.

Immediately preceding initiation of this program, AlN films were grown on GaAs which exhibited high resistivity.[37] An example of typical I-V characteristics is shown in Fig. 13. In this case the current density through the films was less than 10^{-4} amps/cm^2 with 10 V bias across a 1000A AlN film in forward bias (E $\sim 10^6$ V/cm). The current was roughly exponentially dependent on the applied bias. As the growth process was refined and higher purity AlN films were obtained, the films became more conducting (Fig. 14) with the current density at 10 V forward bias increasing by over 3 orders of magnitude. Following installation of the cryopump on the deposition system, the conduction in the AlN films became highly erratic. The films occasionally showed moderate resistivity similar to the films in Fig. 14 but in general were much more conductive at low voltages (1 - 5 V). The AlN/GaAs structures were rectifying. The observation was made that films grown on p-type GaAs substrates showed less conduction than those grown on n-type substrates. Some films showed nonreproducible breakdown and hysteresis in forward bias.

An effort was made to correlate the insulating properties of the films with growth parameters. Several catagories of parameters were investigated. These included parameters related to the surface preparation, the AlN deposition, and the in situ metallization of the structures.

Films with identical AlN preparation variables but with different GaAs surface preparations were examined. These surface preparations were: 1) a Ga_2O_3
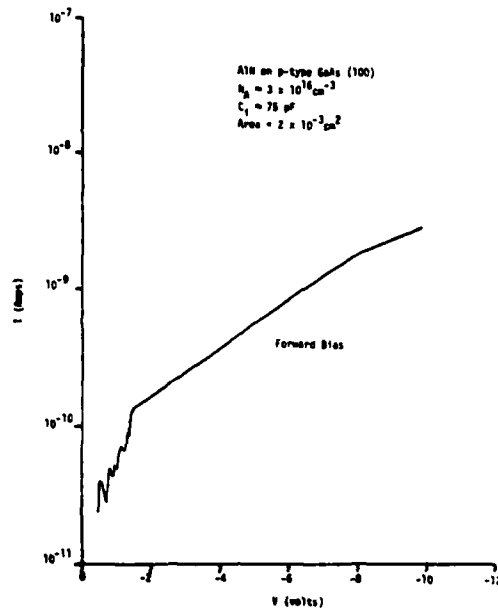
MRDC41116.2FR

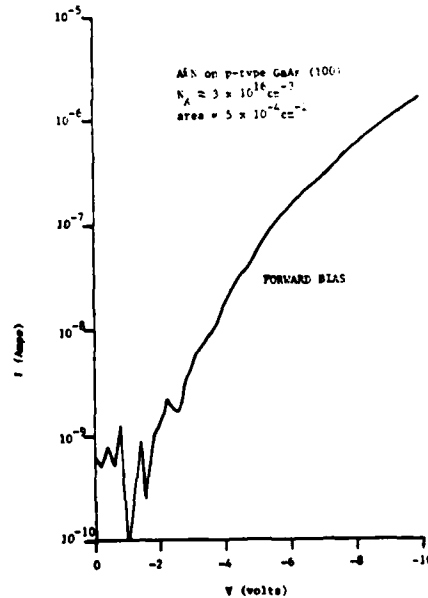Fig. 13 I-V characteristics for an AlN on p-type GaAs (100) MIS capacitor.

Fig. 14 I-V characteristics for an AlN on p-type GaAs (100) MIS capacitor after refinement of growth process.

surface produced by heating the GaAs substrate to 460 - 510°C in situ in the vacuum system,[38] 2) an identical surface heated in NH_3, 3) a thermally cleaned (T > 600°C) GaAs surface, 4) a thermally cleaned GaAs surface heated in an NH_3 flux, and 5) a thermally cleaned GaAs surface heated in an As_4 flux. Each of these surface preparation procedures gave similar results in that there was no discernible difference in the insulating properties of the films.

The AlN deposition parameters were altered to study the influence of deposition temperature and the Al/NH_3 flux ratio on conduction in the AlN films. Again, no discernible difference in the insulating properties of the films was discovered.

Finally, the post-growth metallization procedure was investigated to determine the effect on conduction in the films. It was found possible to evaporate a film of Al over the AlN to prevent oxidation of the surface. Because Al evaporated on the film at elevated temperatures had a grainy morphology, the procedure of allowing the substrate to cool prior to Al deposition was adopted in order to get smooth Al films. During this cooling period in situ AES indicated that the surface developed a thin oxide layer. Further investigations indicated that the presence of this oxide layer substantially affected the electrical transport through the layers. When Al was deposited immediately following growth the films showed substantially higher conductivity than when allowed to cool prior to metallization. Films with the thin oxide layer were prone to electrical breakdown at low voltages. These results and the fact that the electrical resistance of the films degraded following installation of the cryopump indicated that oxygen contamination in the films was most likely responsible for the variation in film conductivity.

It became obvious that the conductivity was high enough in some films to affect the capacitance measurements either by increasing the effective area of the metallic contact or by decreasing the effective thickness of the insulating layer. The model for the structures as MIS diodes, in fact is most likely not appropriate in this case. A more suitable model would be to treat the AlN as a partially depleted semiconductor and the AlN/GaAs interface as a heterojunction. Such a model can qualitatively explain I-V results obtained on

conducting layers (Fig. 15). The layers of AlN for these samples were deposited simultaneously along with an in situ Al metallization step immediately following the AlN growth procedure. The n-type sample shows a very low threshold for forward conduction (< 0.5 V) and a low threshold for reverse bias breakdown ($\sim$ 2 V). The p-type sample does not show reverse breakdown and shows a high threshold for forward conduction (4 - 5 V). These results are consistent with a model of lightly doped n-type AlN deposited on GaAs. The forward and reverse thresholds are further evidence for this interpretation and are consistent with the band offsets estimated by using XPS measurements (Section 4.5).
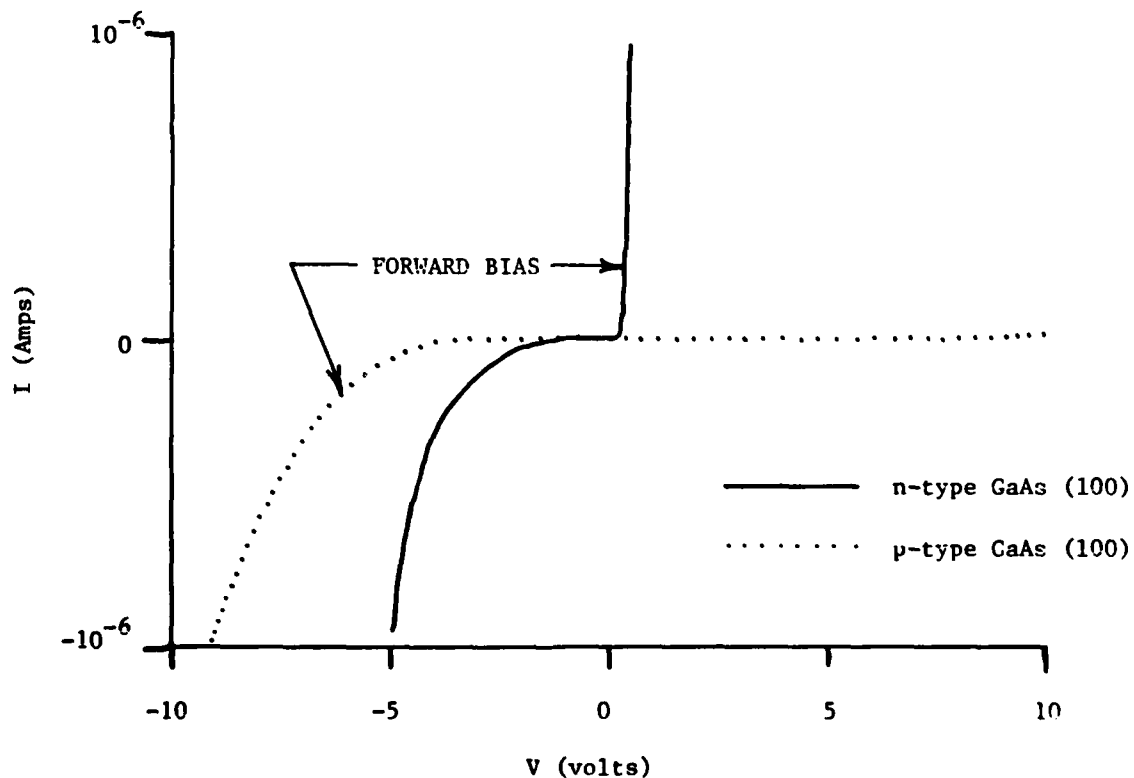

Fig. 15 I-V characteristics of AlN film on n- and p-type GaAs substrates which illustrate heterojunction-like characteristics.

5.3   Analysis of C-V Data

Since the density of interface states on GaAs surfaces can be extremely high, conventional low frequency C-V analysis is difficult. Even high frequency C-V curves show properties which are less than ideal due to the unusually high density of interface states. Hence, great caution must be used in interpreting C-V curves for GaAs MIS structures and the results of such interpretations can only be considered qualitative. Detailed models of the C-V characteristics must include leakage and charge storage effects. It is not always possible to distinguish between charge storage in interface states and charge storage in the insulator.

For the purpose of simplifying the analysis procedure, a simple high frequency model was adopted as shown in Fig. 16. In this model a MIS capacitor fabricated following deposition is modeled as a depletion layer capacitance in series with the capacitance of the insulator. Charging and discharging of interface states leads to a shift in the flatband voltage for which a charge density $Q \approx C_{ins} \Delta V_{FB}$ can be inferred for a given scan rate. The insulator capacitance is estimated from the thickness of the film and the high frequency dielectric constant which is taken to be 8. It is assumed that the emission rate of the interface states is much slower than the measurement frequency (typically 1 MHz).

This type of analysis only applied to a limited number of samples which were measured. However, it was possible to draw a number of conclusions relating charge storage effects to leakage in the film and charging of interface states.

The "best" results obtained in this study are shown in Fig. 17 together with a fit to the simple model just described. The only parameters used to fit the curve are the insulator capacitance and doping level in the substrate.

MODEL FOR C-V FIT
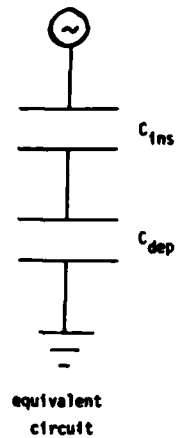
$$\frac{1}{C} = \frac{1}{C_{ins}} + \frac{1}{C_{dep}}$$

$$C_{dep}(\phi) \simeq \sqrt{\frac{q\epsilon_s N_A}{2\phi}}$$

$$V(\phi) = \frac{Q_s(\phi)}{C_{ins}} + \phi$$

ϕ Surface potential

Q_s Semiconductor space charge

C_{dep} Depletion capacitance

C_{ins} Insulator capacitance

C_{ins}

C_{dep}

equivalent
circuit

Fig. 16 Simple model for C-V analysis.

AlN on p-type GaAs (100)
AREA = 5×10^{-4} cm^2

········MODEL
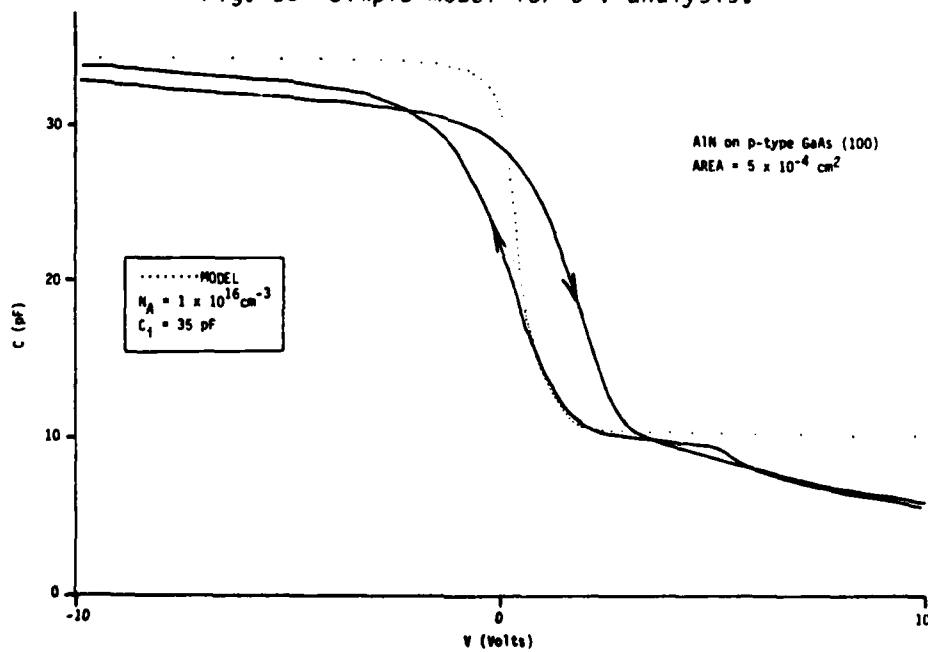$N_A = 1 \times 10^{16}$cm^{-3}
$C_i = 35$ pf

C (pF)

V (Volts)

Fig. 17 C-V plot (1 MHz) for "best" MIS structure. A fit of the data
to the model described in Fig. 16 is also shown.

Questions concerning the results in Fig. 17 are whether the simple model is applicable and whether a reliable inference can be made concerning the density of interface states from the simple model. The model is not applicable if, for instance, the hole emission rate from interface traps is sufficiently high ($\gg$ 1 MHz). The degree of hysteresis can be used to obtain a lower limit on the amount of trapped charge. For the best results charges between 5×10^{11} and 1×10^{12} cm^{-2} were obtained. Such densities of interface states are still far too large for practical devices.

The samples used to obtain C-V curves similar to Fig. 17 where grown fairly early in the course of the program and considerable effort was made 1) to reproduce these results and 2) to improve the interface properties and determine which parameters affect the interface state density. As discussed in Section 5.2 these studies included varying surface preparation, substrate temperature, and the Al/NH$_3$ flux ratio. Simultaneous depositions were normally made on both p- and n-type samples so that C-V characteristics could be established for p- and n-type GaAs with identical deposition conditions. It was not possible to provide a definitive correlation between any of the deposition parameters and the interface state charge density obtained by using the simple analysis procedure described previously in this section.

As described in Section 5.2, the films showed increased conduction as the deposition process was refined and a cryopump was installed on the growth chamber. This increase in conduction made C-V analysis impossible because the MIS devices would excessively load the C-V measurement apparatus. Typical C-V curves for two different cases of high leakage and of low breakdown voltage are shown in Figs. 18 and 19, respectively. In the high leakage case (Fig. 18) very low hysteresis is observed, however, the "insulator capacitance" is much larger than expected for this film thickness. The only way to explain the behavior of the films in this case is to assume that the effective area of the MIS devic~ is substantially larger or the effective thickness of the film is substantially lower than optically determined. This interpretation is consistent with the I-V properties of the films described previously and the heterojunction model described in Section 5.2.
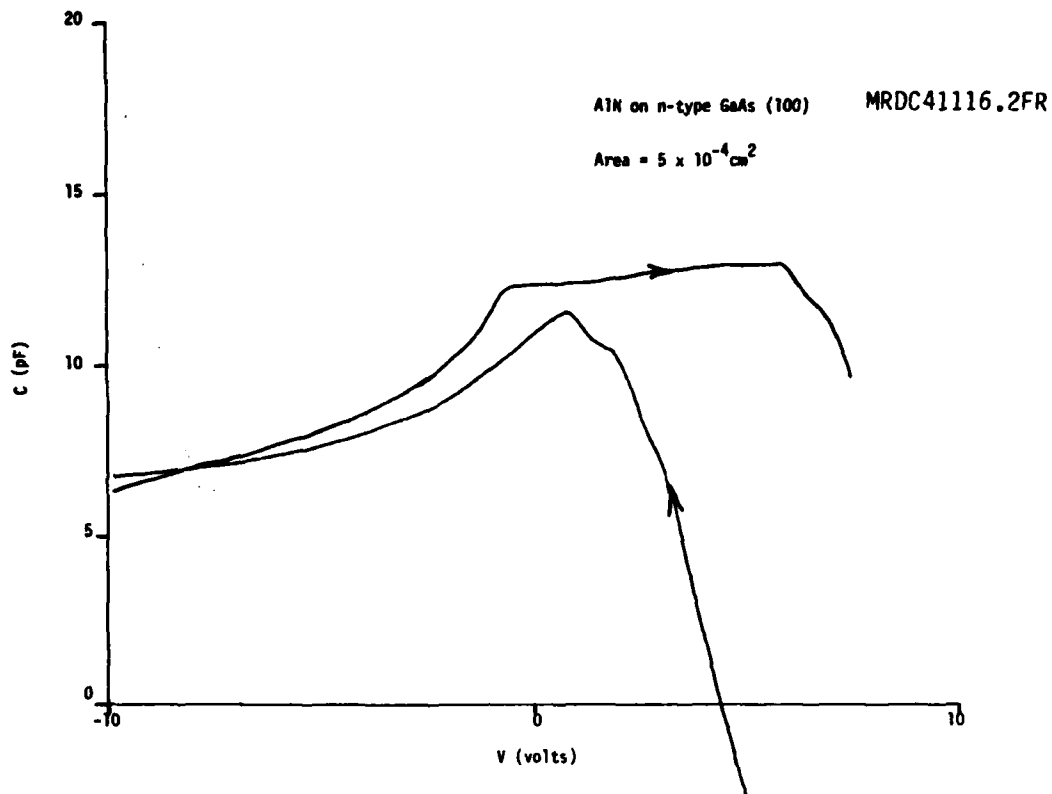
Fig. 18 C-V plot for AlN/GaAs sample which exhibited high leakage.
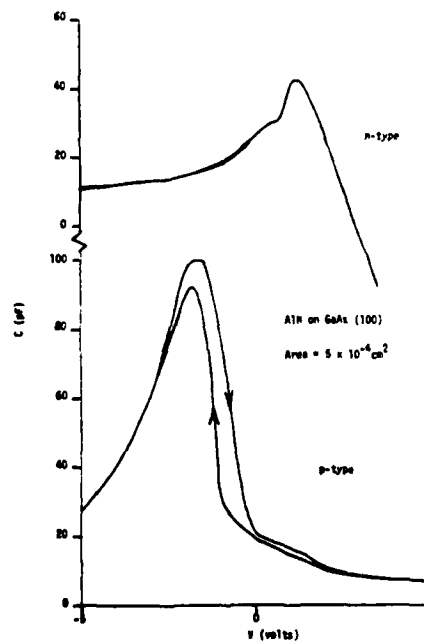

Fig. 19 C-V plots for AlN films on n- and p-type GaAs which
exhibited low breakdown voltage.

Very little hysteresis was observed in the high leakage films. Al-
though this might be interpreted to indicate that such films have lower inter-
face state densities, a more likely explanation is that the time constant assoc-
iated with trapping of charge in the films and at the AlN/GaAs interface has
become short enough that hysteresis is not observed.

In each case when the properties of AlN/p-GaAs structures were compared
with AlN/n-GaAs structures, it was found that the capacitance of the n-type
structures was substantially below the insulator capacitance. This low value
was consistent with Fermi level pinning ~ 0.7 eV below the conduction band edge
which is in accord with previous studies of deposited dielectrics on GaAs. The
capacitance of AlN/p-GaAs structures was equal to the insulator capacitance in
accumulation at frequencies < 10 MHz. However, at 10 MHz the capacitance was
found to decrease suggesting that a large density of fast interface states
occurred in these structures.

5.4   DLTS Measurements

On some samples DLTS measurements were attempted to investigate
interface state distributions. These samples were typical of those which
exhibited the "best" C-V properties as described in Section 5.3.

The basic technique is an adaptation of DLTS as suggested by Lang;[39]
DLTS is widely used to detect deep defect levels in bulk materials. To study
interface states, a MIS structure is used. During a large forward bias voltage
pulse, the device is driven into accumulation which fills the states at the
interface with electrons. Following this pulse, the device is reverse-biased
into deep depletion. The release of charge from the interface is measured by
observing the corresponding change in capacitance of the device.

The method used relies on the strong temperature dependence of the
emission rate and is more appropriate for GaAs because it is less sensitive to
dispersion and hysteresis effects. With this method and for a distribution of
states $N_{ss}(E)$ with a capture cross-section $\sigma(E,T)$, the released charge is

$$\Delta Q = q \int_{-\infty}^{\infty} N_{ss}(E) \left(\exp(-t_1/\tau) - \exp(-t_2/\tau) \right) dE \quad . \tag{1}$$

For given values of t_1 and t_2, it can be shown[40] by using Eq. (1) that

$$\Delta Q = AkT \, N_{ss}(E_{max}) \quad , \tag{2}$$

where A is a constant and where $E_{max} = kT \ln(\sigma v_{th} N_c \tau)$. It has been assumed that $\sigma(E)$ and $N_{ss}(E)$ are relatively constant with respect to energies within kT of E_{max}.

To obtain reliable results by using this method, it is necessary to drive the semiconductor surface into strong accumulation and to correct for changes in the capacitance so the charge ΔQ can be reliably determined. For large interface state densities it becomes difficult to drive the semiconductor into accumulation.

For the devices which were measured, it was not possible to drive the surface into accumulation at low temperatures. The DLTS spectra obtained between 77K and 350K were extremely broad and difficult to interpret. The fact that large hysteresis and capacitance transients were observed at lower temperatures is further evidence that a large density of interface states remains following AlN deposition.

6.0 MISFET DEVELOPMENT

A number of studies were performed in order to define a process technology for AlN MISFET's. To be suitable for device applications AlN/GaAs structures must be able to survive ordinary semiconductor device processing. In this case the AlN films must be patterned by photolithography, ion-implanted, annealed, metallized, and etched in controllable fashions. Such a process technology is necessary for any device fabricated by using AlN as a dielectric layer whether the layer is simply used as a cap, or is used as part of the device as with a MISFET or surface acoustic wave device.

To be a practical device element, a GaAs MISFET must be an enhancement mode n-channel device in order to have an advantage over current MESFET designs. A GaAs MISFET would operate with large voltage swings and higher noise margins than conventional enhancement mode n-channel MESFET devices. In addition the threshold voltage would be far less critical than with normal enhancement mode MESFET DCFL logic gates because of the larger voltage swing.

6.1   Approach

The first approach tried was to fabricate a self-aligned gate enhancement mode GaAs MISFET by using the process shown in Fig. 20. An AlN/GaAs structure was grown as described in Section 3.7. A refractory metal was deposited and patterned to define a gate (Fig. 20-2). An n^+ implant was masked by the gate region to form a self-aligned structure. The structure was annealed to activate the implant (Fig. 20-3). To complete the device, ohmic contacts were defined by etching holes in the AlN. An ohmic metal layer was deposited and patterned by lift-off. The metallization was alloyed with the GaAs by using a conventional ohmic alloy procedure.

Processing problems developed with this first approach and consequently the procedure was changed to a non-self aligned gate process which utilized a more established approach and eliminated the need for high temperature processing of the metal gate. This second approach is shown schematically in Fig. 21.

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1. GROWTH
   a. AℓN growth
   b. Metal deposition
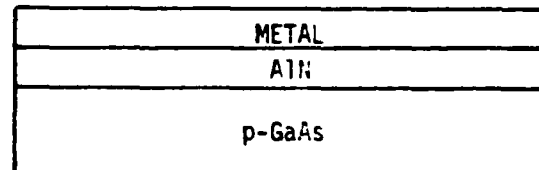
| METAL |
| AlN |
| p-GaAs |

2. GATE DEFINITION
   a. Photolithography
   b. Etch
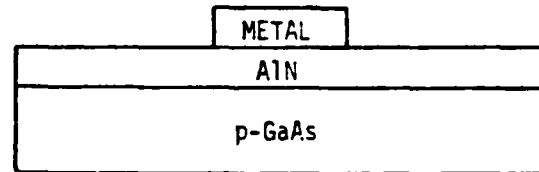
| METAL |
| AlN |
| p-GaAs |

3. IMPLANT
   a. Photolithography
   b. Implant
   c. Strip
   d. Anneal

	METAL	
	AlN	
n		n
	p-GaAs	

4. OHMIC DEFINITION
   a. Photolithography
   b. Etch
   c. Evaporation
   d. Lift-Off
   e. Alloy

METAL	METAL	METAL
	AlN	
n+	n	n	n+
	p-GaAs	
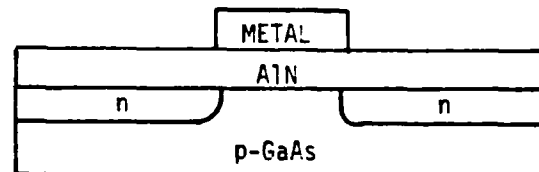
Fig. 20 Self-aligned gate MISFET process.

MRDC41116.2FR

1. GROWTH

   a. AℓN Growth

AℓN
p–GaAs

2. IMPLANT

   a. Photolithography
   b. Implant
   c. Strip
   d. Anneal

3. OHMIC DEFINITION

   a. Photolithography
   b. Etch
   c. Evaporation
   d. Lift-off
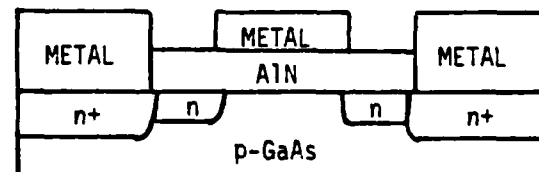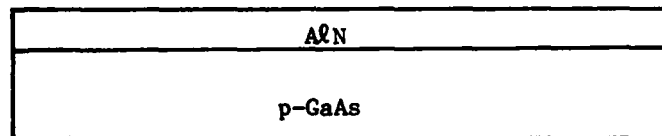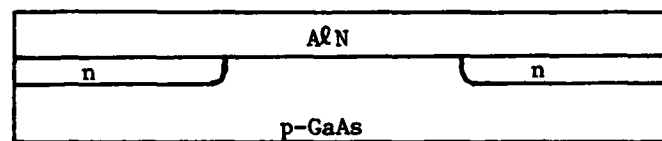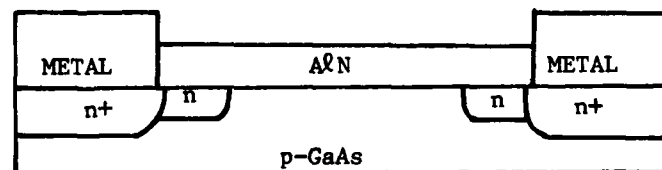   e. Alloy

4. GATE DEFINITION

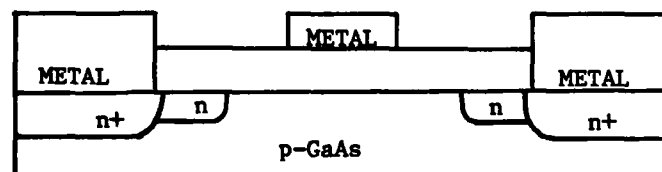   a. Photolithography
   b. Metal Deposition
   c. Lift-off

Fig. 21 MISFET fabrication process.

With the second approach, alignment marks were first produced by lightly etching the AlN with dilute HF following photolithography. A second photolithographic step defined a selective implant. The sample was implanted, the resist was stripped and the sample was annealed to activate the implant. An ohmic metallization pattern was defined by photolithography, a hole was etched in the AlN and metal was deposited and defined by liftoff. The ohmic contact was formed by alloying. To complete the devices, a metal gate was defined by photolithography and lift-off.

By using the self-aligned gate approach described above, it was possible to fabricate simple gated diode structures. With the second approach it was possible to fabricate FET structures with 1 micron dimensions. In the following sections this fabrication is described in more detail with emphasis on the major process steps and problems encounterd in processing AlN.

6.2   Mask Set

The initial effort to fabricate AlN/GaAs MISFETs attempted to use an existing MESFET mask set (used for digital IC fabrication) together with Censor 10X projection mask alignment. Acceptable alignment marks could not be obtained for use with the Censor. The alignment marks must survive high temperature anneals and still be recognizable to the sensing circuitry of the Censor. In addition, the underlying film must be relatively nonreflecting compared to the alignment mark. The normal alignment mark metallization (Ti) reacted with the AlN when annealed and hence could not be used.

An alternate mask set which had been developed for use with microwave circuits was obtained. Because this mask set used contact alignment and was manually operated, the alignment difficulties were eliminated. A difficulty was encountered with the sensitivity of the deposited AlN films to photoresist developer. It was found that recently deposited films had a tendency to dissolve in standard AZ photoresist developing solutions. The reactivity of the films decreased with time following exposure to the atmosphere. The reaction of the AlN films to form a protective native oxide surface may explain these results.

Unfortunately, this reactivity made it difficult to control the photolitho-
graphic processes.

To produce alignment marks photoresist was deposited and developed by
using standard techniques and the AlN was etched lightly in dilute HF to form
alignment patterns. Since no metal was involved, these alignment marks were
able to survive the anneal procedure following ion implantation. The contrast,
however, was insufficient to use the Censor for alignment purposes.

6.3 Ion Implantation

The use of AlN as an ion implantation cap has been previously estab-
lished. To evaluate reactively deposited AlN as an implantation cap a standard
ion implantation procedure (used to evaluate material for GaAs IC production)
was performed. The procedure was 1) to deposit AlN as described, 2) implant the
GaAs through the AlN capping layer, 3) anneal the GaAs at 850°C in hydrogen for
30 min, and 4) obtain a C-V profile by using an evaporated C-V pattern with a
large and small area contact. The large area contact acts as a pseudo-ohmic and
eliminates the need for an extra metallization step. The results of this proce-
dure, Fig. 22, indicated a sharper profile than obtained by using a Si_3N_4 cap
with activation efficiencies near 100% as well as could be determined. The
range of the implant is likely to be similar to Si_3N_4.

Annealing of the implant was found to be accompanied by a change in the
surface morphology which produced a hazy appearance. In order to maintain the
integrity of the film through the anneal process, it was necessary to use a
rapid anneal cycle. Several experiments with rapid thermal annealing on ion
implanted samples were performed which demonstrated that good surface morphology
suitable for further processing could be obtained.

The initial approach was to develop a self-aligned gate GaAs MISFET
device process. To use this type of process it was necessary to anneal the
sample with gate metallization in place. The use of Ti, Ti-W, and W metalliza-
tions to produce this type of structure was attempted. Ti was found to react
with the AlN films, whereas W exhibited poor adhesion to AlN and tended to peel
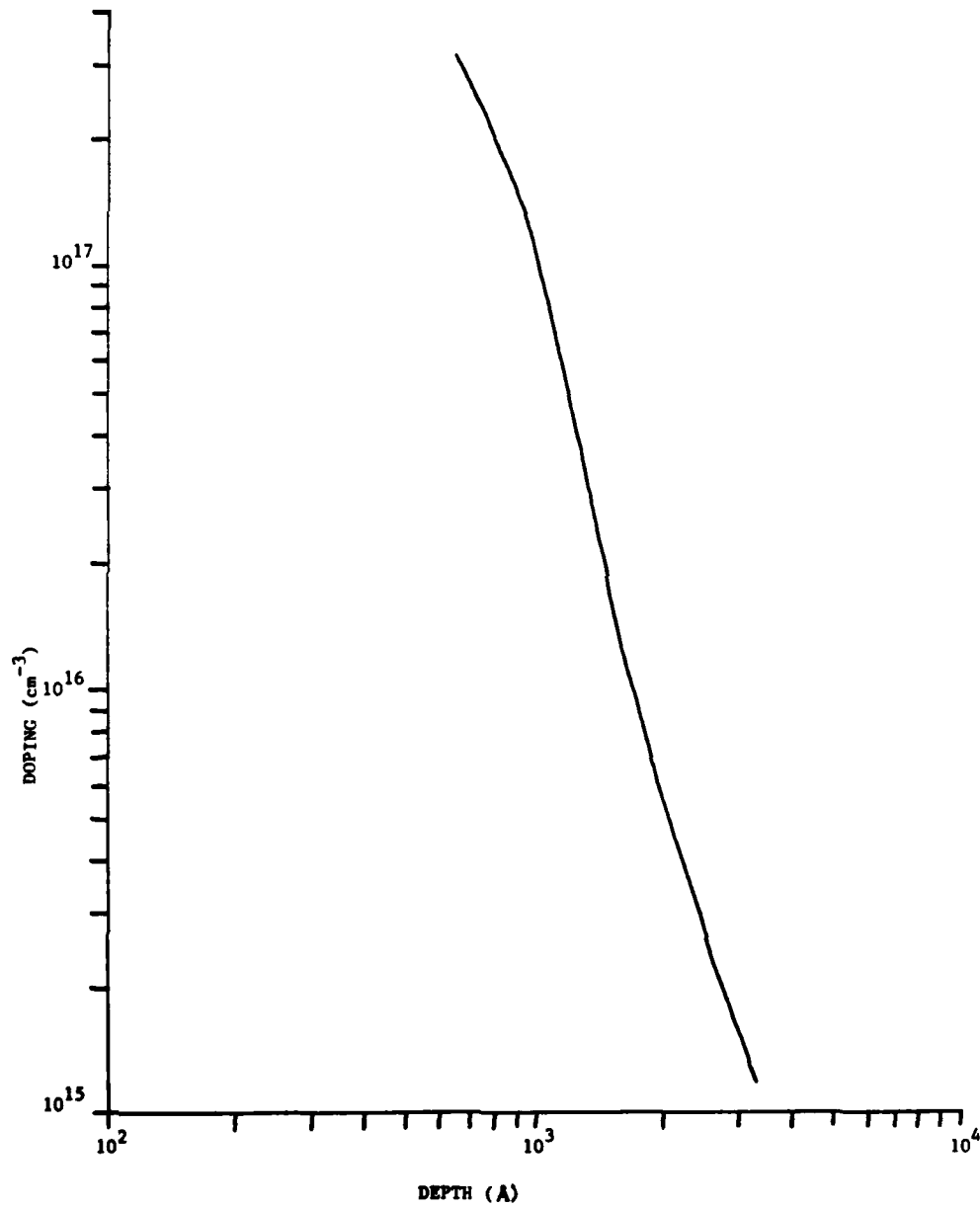
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Fig. 22 Ion implantation doping profile obtained by using
AlN capping layer.

at thicknesses greater than a few hundred Angstroms or when heated. No metals were found which would stick to the AlN and also survive the annealing following ion implantation.

As a result the non-self-aligned gate approach was chosen because no high temperature anneal was necessary with metal on the wafer.

6.4   Etching and Formation of Metal Contacts

Following the alignment mark registration step and ion implantation and annealing steps, it was necessary to produce ohmic contacts to the drain and source regions. This step required photolithographic definition of the contact, etching of the AlN, metallization, a lift off of the metal, and an ohmic alloy step. The etching of the AlN was the most critical and most difficult step to control. Since no known process is available for dry etching of AlN, it was necessary to use a wet etch process which was sensitive to both temperature and device geometry. Warm H_3PO_4 was used to etch the AlN. This wet etch process was highly susceptible to undercutting the photoresist which altered the device geometry. When 1 micron geometries are used this step is a low yield process.

Following the etching procedure AuGe/Ni was deposited to form a metal layer roughly 1000A thick. The metal was lifted to define the FET source and drain contacts. These contacts were alloyed in H_2 gas at 450°C for 5 min to produce the ohmic contacts.

6.5   Gate Metallization

The final step in the process was the gate metallization. Following photolithography, Ti-Au was deposited to form a gate metal layer and lifted to define 1 micron long gates for the MISFET's. A photograph of a finished MISFET test structure is shown in Fig. 23. The source (S), gate (G), and drain (D) probe pads are indicated in the figure.

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Fig. 23   Photograph of AlN/GaAs MISFET test structure. Source, gate and drain
          probe pads are labeled S, G and D, respectively. Magnification is 95X.

6.6   Electrical Measurements

Both gated diode and MISFET devices were fabricated as described in Section 6.1. The gated diode was a self-aligned structure on semi-insulating material with W gate metallization. In such a structure one expects to observe a large increase in the high frequency capacitance when inversion is obtained. No substantial change in capacitance was observed over the voltage range -10 to 10 V.

The MISFET structures shown in Fig. 23 were measured for three different wafers. The results for each structure were similar. Typical drain-source

current (I_{DS}) vs drain-source voltage (V_{DS}) characteristics are shown in Fig. 24. In this figure the gate voltage (V_G) ranges from -5 to 0 volts. The modulation of I_{DS} is 3 orders of magnitude less than expected for an ideal MISFET structure and the direction of the modulation is opposite to what would be expected. Careful inspection of the device characteristics indicated that under some circumstances, this modulation was associated with gate leakage currents.
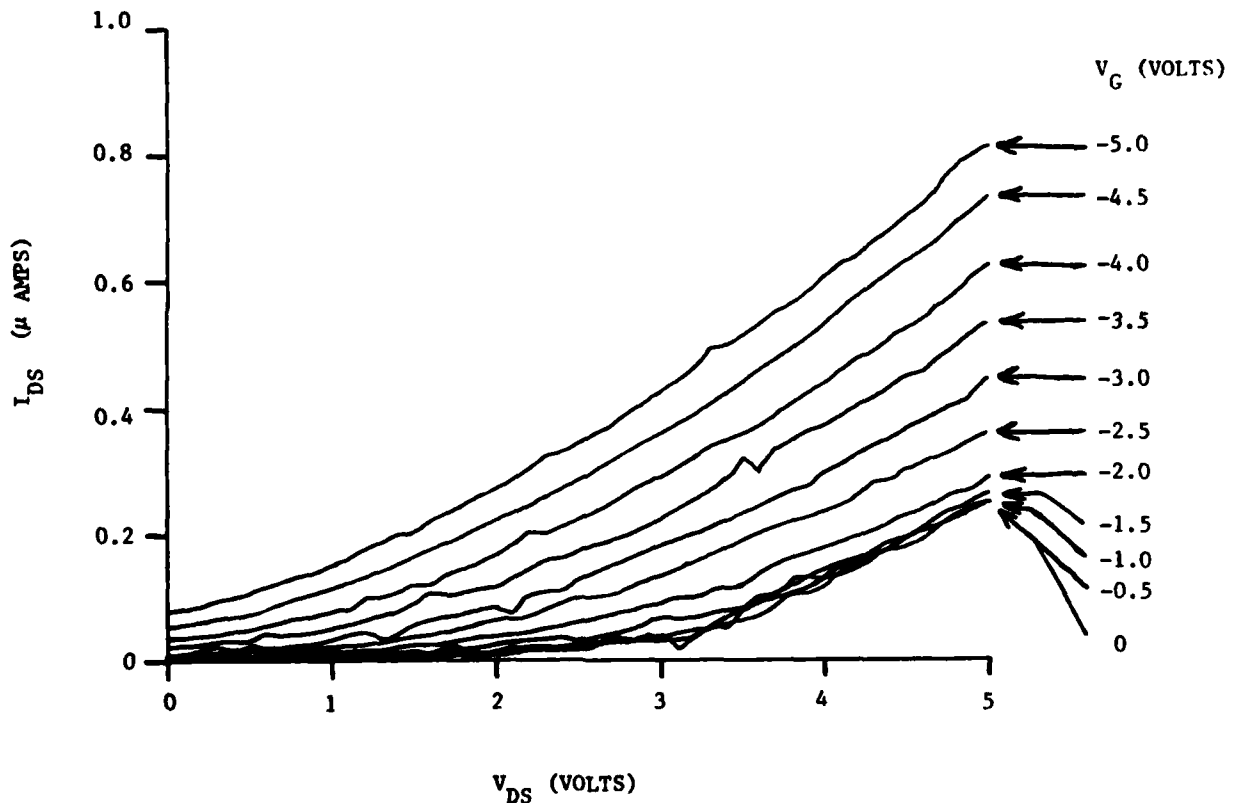

Fig. 24 I_{DS} vs V_{DS} for several values of V_G.

It was concluded from the gated diode and MISFET measurements that inversion was not achieved in these test structures. These results are consistent with the presence of a large density of interface states at the AlN/GaAs interface.

7.0 SUMMARY

The use of AlN as the gate insulator for GaAs MIS applications was investigated. Recent studies have provided strong support of a defect model for Fermi level pinning at GaAs and other III-V semiconductor interfaces. The large densities of interface states which have frequently prohibited development of a practical GaAs MIS technology may be associated with the same defects which cause Fermi level pinning. The possibility of using a wide bandgap isoelectronic III-V material (i.e., AlN) to minimize GaAs interface states associated with characteristic defects and impurites was explored.

Reactive evaporation was utilized to prepare AlN films on heated GaAs substrates. The films were grown in a UHV (low 10^{-9} Torr base pressure) system. An NH_3 effusion cell and an Al MBE source provided the reactants for AlN growth. Several material preparation variables were investigated which included choice of substrate material, substrate surface preparation, *growth temperature*, Al/NH_3 flux ratio, and deposition rate. The optimum AlN film growth parameters in terms of morphology and adhesion involved thermal cleaning of the GaAs substrate, utilizing a 500-550°C substrate growth temperature, providing an effective NH_3 partial pressure of 5×10^{-5} to 1×10^{-4} Torr at the GaAs surface, and adjusting the Al flux to obtain a growth rate of approximately 100./min.

The AlN films were characterized by several techniques. AES performed _in situ_ established that oxygen and carbon contamination was below the detectability limit. AES, x-ray diffraction, TEM, and far infrared transmission confirmed that the films consisted of essentially stoichiometric AlN with the hexagonal wurtzite type of crystal structure.

The insulating properties of the AlN/GaAs structures appeared to depend on preparation conditions. Possible correlations with parameters which included surface preparation, AlN deposition conditions, and _in situ_ metallization were examined. It was concluded that undetected residual oxygen contamination in the AlN films was most likely responsible for the observed variations in film conductivity.

Complex C-V results were obtained for most AlN/GaAs MIS structures. The results were undoubtedly influenced by large densities of interface states, leakage, and charge storage effects. In some favorable cases it was possible to model the MIS capacitor as a depletion layer capacitance in series with the insulator capacitance. Although the C-V analysis based on this model was not unambiguous, the results suggested interface state charge densities between 5×10^{11} and 1×10^{12} cm^{-2}. No definitive correlation between AlN/GaAs preparation parameters and interface state charge densities was obtained. It was observed that very little hysteresis was associated with high leakage films most likely due to short time constants for trapping of charge in the films and at the AlN/GaAs interface. A comparison of forward bias C-V results for AlN/n-GaAs and AlN/p-GaAs structures suggested mid-gap Fermi level pinning.

Processes were developed to fabricate both gated diodes and MISFET's from AlN/GaAs samples. Electrical measurements on both devices provided no indication that inversion was achieved. These results were again consistent with the presence of large interface state densities in the AlN/GaAs samples.

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9.0 REFERENCES

1. C.W. Wilmsen and S. Szpak, Thin Solid Films, 46, 117 (1977).

2. B.L. Sharma, Solid State Technol. 48, 122 (1978).

3. Special issue, Thin Solid Films 56, No. 1 and 2 (1979).

4. H.H. Wieder, J. Vac. Sci. Technol. 15, 1498 (1978).

5. W.E. Spicer, I. Lindau, P. Skeath and C.Y. Su, J. Vac. Sci. Technol. 17, 1019 (1980).

6. R.H. Williams, J. Vac. Sci. Technol. 18, 929 (1981).

7. R.W. Grant, J.R. Waldrop, S.P. Kowalczyk and E.A. Kraut, J. Vac. Sci. Technol. 19, 477 (1981).

8. H.C. Casey, Jr., A.Y. Cho and E.H. Nicollian, Appl. Phys. Lett. 32, 678 (1978).

9. W.T. Tsang, M. Olmstead and R.P.H. Chang, Appl. Phys. Lett. 34, 408 (1979).

10. F.H. Eisen, B.M. Welch, H.M. Uller, R. Gamo, T. Inada and J.W. Mayer, Solid State Electron. 20, 219 (1977).

11. S. Okamura, H. Nishi, T. Inada and H. Hashimoto, Appl. Phys. Lett. 40, 689 (1982).

12. T.L. Chu, D.W. Ing and A.J. Noreika, Solid State Electron. 10, 1023 (1967).

13. H.M. Manasevit, F.M. Erdmann and W.I. Simpson, J. Electrochem. Soc. 118, 1864 (1971).

14. W.M. Yim, E.J. Stofko, P.J. Zanzucchi, J.I. Pankov, M. Ettenberg and S.L. Gilbert, J. Appl. Phys. 44, 292 (1973).

15. T.L. Chu and R.W. Kelm, J. Electrochem. Soc. 122, 995 (1975).

16. S. Zirinsky and E.A. Irene, J. Electrochem. Soc. 125 305 (1978).

17. M. Morita, S. Isogai, N. Shimizu, K. Tsubouchi and N. Mikoshiba, Jpn. J. Appl. Phys. 20, L173 (1981).

18. A.J. Noreika, M.H. Francombe and S.A. Zeitman, J. Vac. Sci. Technol. 6, 194 (1969).

19. S. Mirsch and H. Reimer, Phys. Status Solidi A 11, 631 (1972).

20. P.N. Favennec, L. Henry, T. Janicki and M. Salvi, Thin Solid Films 47, 327 (1977).

21. H. Birey, S.-J. Pak and J.R. Sites, Appl. Phys. Lett. 35, 623 (1979).

22. T. Shiosaki, T. Yamamoto, T. Oda and A. Kawabata, Appl. Phys. Lett. 36, 643 (1980).

23. E.V. Gerova, N.A. Ivanov and K.I, Kirov, Thin Solid Films 81, 201 (1981).

24. J.J. Hantzpergue, Y. Pauleau and H.C. Remy, Thin Solid Films 75, 167 (1981).

25. A Fathimulla and A.A. Lakhani, J. Appl. Phys. 54, 4586 (1983).

26. M.T. Wauk and D.K. Winslow, Appl. Phys. Lett. 13, 286 (1968).

27. S. Yoshida, S. Misawa and A. Itoh, Appl. Phys. Lett. 26, 461 (1975).

28. S. Winsztal, B. Wnuk, H. Majewska-Minor and T. Niemyski, Thin Solid Films 32, 251 (1976).

29. S. Yoshida, S. Misawa, Y. Fujii, S. Takada, H. Hayakawa, S. Gonda and A. Itoh, J. Vac. Sci. Technol. 16, 990 (1979).

30. H. Yamashita, K. Fukui, S. Misawa and S. Yoshida, J. Appl. Phys. 50, 896 (1979).

31. F. Alexandre, J.M. Mason, G. Post and A. Scavennec, Thin Solid Films 98, 75 (1982).

32. Powder Diffraction File, 25-1133, JCPDS International Center for Diffraction Data, Swarthmore, Pennsylvania, 1982.

33. E.A. Kraut, R.W. Grant, J.R. Waldrop and S.P. Kowalczyk, Phys. Rev. B 28, 1965 (1983).

34. J. Hedman and N. Martensson, Physica Scripta 22, 176 (1980).

35. A.T. Collins, E.C. Lightowlers and P.J. Dean, Phys. Rev. 158, 833 (1967).

36. H. Nishi, S. Okamura, T. Inada, H. Hashimoto, T. Katoda and T. Nakamura, Inst. Phys. Conf. Ser. N63, 356 (1982).

37. K.R. Elliott and R.W. Grant, unpublished data.

38. R.W. Grant, S.P. Kowalczyk, J.R. Waldrop and W.A. Hill, in "The Physics of MOS Insulators," p. 202 (Pergamon Press, N.Y., 1980) edited by G. Lucousky, S.T. Pantelides and F.L. Galeener.

39. D.V. Lang, J. Appl. Phys. 45, 3104 (1974).

40. M. Schulz and N.M. Johnson, Solid State Comm. 25, 481 (1978).

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